



UNITED STATES PATENT AND TRADEMARK OFFICE

48
UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 09/429,283 | 10/28/1999 | SHUICHI UENO | 0057-2534-2Y | 5740 |

7590

10/02/2002

OBLON SPIVAK MCCLELLAND MAIER & NEUSTADT
FOURTH FLOOR
1755 JEFFERSON DAVIS HIGHWAY
ARLINGTON, VA 22202

EXAMINER

FOURSON III, GEORGE R

| ART UNIT | PAPER NUMBER |
|----------|--------------|
|----------|--------------|

2823

21

DATE MAILED: 10/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

MAILED

OCT 02 2002

GROUP 2800

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Paper No. 21

Application Number: 09/429,283
Filing Date: October 28, 1999
Appellant(s): UENO ET AL.

Robert C. Mattson
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 5/20/02.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is substantially correct. The changes are as follows: The rejection of claims 14-27 is under 35 U.S.C. § 103(a) and is based on "Kuroi et al" rather than "Kurol et al".

(7) Grouping of Claims

Appellant's brief includes a statement that claims 14-15, 16-18 and 19-27 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

Art Unit: 2823

(9) Prior Art of Record

| | | |
|-------------|---------------|---------|
| JP 4-157766 | Sony Corp. | 5-1992 |
| 6,004,849 | Gardner et al | 12-1999 |
| 5,780,330 | Choi | 7-1998 |

Chou, A.I., "The Effects of Nitrogen Implant into Gate Electrode on the Characteristics of Dual-Gate MOSFETs with Ultra-thin Oxide and Oxynitrides", IEEE (August 4, 1997) pp.174-177

Kuroi, T., et al., "The Impact of Nitrogen Implantation into Highly Doped Polysilicon Gates for Highly Reliable and High-Performance Sub-Quarter-Micron Dual Gate Complementary Metal Oxide Semiconductor",

Japanese Journal of Appl. Phys., Vol.34 (February 1995), pp.771-775 493 94

Sze, S.M., "VLSI Technology", second edition, McGraw Hill (1988)

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 14-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Japanese Patent 4-157766, Gardner et al '849, Choi '330, Chou et al (1997 IEEE), Kuroi et al (J. Appl. Phys. 1995) and Sze.

Japanese Patent 4-157766 discloses formation of a field oxide isolated P-channel transistor including selective implantation of nitrogen into the polysilicon layer later patterned to form the gates of a p-

Art Unit: 2823

channel transistor having nitrogen in the lower portion of the gate and an n-channel transistor having no nitrogen in the gate (abstract and figures 1A-1C).

Choi discloses blanket p-type doping of a polysilicon layer 200 followed by selective doping of layer 200 in region 112 followed by patterning of the layer to form gates 208a-d such that the gates of all transistors formed in region 112 would contain p-type dopant due to the blanket implantation (fig 3a-3c). The reference discloses that nitrogen implantation can be combined with such a process (col.8, lines 16-18).

Gardner et al discloses the dependence of threshold voltage on concentration of dopant in the gate of a MOSFET and the formation of MOSFET's having different concentrations of dopant on the same wafer thus establishing dopant concentration in the gate of a MOSFET to be a result effective variable (col.10, lines 19-26 and col.12, lines 1-11)(MPEP 2144.05). The reference discloses forming a photoresist layer to cover any or all of the gate to adjust the threshold voltage and that it might be desirable to form MOSFETs in critical signal paths to have a lower threshold voltage than other MOSFETs in the circuit (col.10, lines 20-25) and that although one device has been shown it is understood that in actual practice many devices are fabricated on a single semiconductor wafer as is widely practiced in the art (col.12, lines 1-11).

Chou et al discloses the effects of different concentrations of nitrogen in the gate of a MOSFET with respect to B, which is a p-type dopant and As, which is an n-type dopant, thus establishing nitrogen concentration in the gate of a MOSFET to be a result effective variable for both p-type and n-type gates and thereby disclosing the suitability of combining nitrogen concentration with dopant concentration in a gate of a MOSFET for both p-type and n-type gates (Chou et al, introduction).

Kuroi et al discloses the effects of different nitrogen concentrations and dopant concentrations in the gate of a MOSFET for both p-type and n-type gates thus establishing concentrations of dopant and nitrogen together to be a result effective variable (see Fig.2,3 and 9).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Japanese Patent 4-157766 and Choi '330 to enable doping of the polysilicon layer of Japanese Patent 4-157766 in the p-channel area and to further combine the teachings of the references with those of Gardner et al to enable formation of circuits having a desired characteristic including formation of MOSFET's having different concentrations of dopant in the gates on the same wafer. The selective introduction of particular dopant and nitrogen concentrations in the gates of the MOSFET's so produced, including formation of MOSFET's having more than 2 different concentrations of nitrogen would have been a matter of routine optimization in view of the teachings of Chou et al and Kuroi et al that these are individually and/or in combination result effective variables and in view of Gardner that the choice depends on the desired device characteristics. In such a process, all transistor gates in a region corresponding to region 112 of Choi '330 would contain the same concentration of p-type dopant due to the blanket implantation and some transistor gates would contain additional dopant and/or nitrogen due to the selective implantation. Furthermore, the claims are open to the amounts of dopant in the gates differing to an extent that is insufficient to substantially alter the device performance as compared to a device having all gates doped equally.

With respect to claim 14, Choi is relied on as teaching selective doping of a polysilicon layer used to form gates of MOSFETs with a conductive impurity in addition to the teachings of the additional references relied on including those related to selective nitrogen implantation and routine optimization of the nitrogen and dopant concentrations in the gates.

With respect to claim 16, Japanese Patent 4-157766 is relied on as teaching selective implantation of nitrogen into a polysilicon layer used to form gates of MOSFETs in addition to the teachings of the additional references relied on including those related to formation of n-type and p-type gates and routine optimization of the nitrogen concentrations in the gates. See claim 19, line 13, for indication that "transistor" does not require a fully formed transistor.

With respect to claim 19, Japanese Patent 4-157766 is relied on as teaching selective implantation of nitrogen into a polysilicon layer used to form gates of MOSFETs in addition to the teachings of the additional references relied on including those related to doping a polysilicon layer used to form gates of MOSFETs and routine optimization of the nitrogen concentrations in the gates.

(11) Response to Argument

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The arguments that the references contain teachings in addition to those relied on do not negate the teachings relied on. For example, the specific method of forming a field effect transistor disclosed by Gardner is not relied on in the rejection and does not negate the relied on teaching of forming MOSFETs having different threshold voltages on the same wafer.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill

Art Unit: 2823

in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, all references are drawn to MOSFET formation and are thus analogous.

Japanese Patent 4-157766 is not relied upon as teaching implanting nitrogen into different gates at different non-zero amounts but instead for the teaching of selective implantation of nitrogen into a transistor gate material.

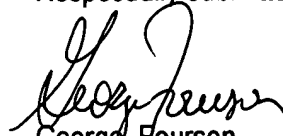
Applicant argues that Gardner et al does not disclose formation of plural devices. However, the reference discloses forming a photoresist layer to cover any or all of the gate to adjust the threshold voltage and that it might be desirable to form IGFET's in critical signal paths to have a lower threshold voltage than other IGFET's in the circuit (col.10, lines 20-25) and that although one device has been shown it is understood that in actual practice many devices are fabricated on a single semiconductor wafer as is widely practiced in the art (col.12, lines 1-11).

In response to applicant's argument regarding Chou, the reference is not relied on as teaching implanting dopant into different gates at different non-zero amounts but instead for the teaching of the effects of different dopant concentrations on MOSFET performance.

Art Unit: 2823

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,



George Fourson
Primary Examiner
Art Unit 2823

GFourson
September 24, 2002

Conferees
Matthew Smith *MS*
Wael Fahmy *W.F.*

OBLON SPIVAK MCCLELLAND MAIER & NEUSTADT
FOURTH FLOOR
1755 JEFFERSON DAVIS HIGHWAY
ARLINGTON, VA 22202

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800